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EXAMINER	
PAN, DANIEL H	
ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/644,337	Applicant(s) WOLRICH ET AL.	
	Examiner Daniel Pan	Art Unit 2183	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) ____ is/are withdrawn from consideration.

5)☐ Claim(s) ____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) ____ is/are objected to.

8)☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on ____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. ____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date ____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. ____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: ____.

1. Upon the newly amended feature of hardware based multiprocessor, a new ground of rejection ahs been applied. Panwar et al. (5,838,988) is used to show the hardware based multithreaded processing (see action below). All references have been cited on record except Panwar (5,838,988). Panwar (5,838,988), now has been cited.

2. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection. However, the response to applicant's remarks is included herein to clarify the teaching of the art of record.

3. As to applicant's remark on LeBlanc describing the software based system, see the reasons of obviousness of LeBlanc et al. (5,542,070) in view of Panwar et al. (5,838,988) in the action below.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1, 14, 21, 29, 30 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons are given below.

5. As to claim 1, no substantial practical application can be found in the claim. Although claim recites pushing/popping datum into/off the stack by the processing thread, the practical application of the push and popping is not found in claim 1. The pushing and popping is the intended use, and not positive limitations. The focus is not on the features or steps taken to achieved a final result which is useful, concrete, and tangible, but rather the final result achieved is useful, concrete, and tangible (see MPEP 2100).

6. As to the newly amended feature of the hardware-based multi-threaded processor and the computer instructions that perform a task, examiner holds that the hardware –based multi-threaded processor is an intended use, and is a generic arrangement of the processor. No details of the hardware that impart the functionalities of the processor can be found in the claim. As to the computer instructions that perform a task, no components of the instructions can be found to impart the functionalities of the task can be found. Furthermore, practical application of the task is not clear. The final result of the task is unclear.

7. As to claim 14, although claim recites a stack module that store data and first processing thread for pushing and second processing thread for popping, no substantial practical application can be found for the stack module that stores data and the first/second processing threads. It is directed to generic arrangement of the system parts, not parts in a machine with particular use. No particular use can be found with a machine because the practical application for pushing and popping is not clear. As to the newly amended features of claim 14, claim 14 has been amended with similar features. Therefore, similar analysis in Paragraph 4 above can be done, and render claim non-statutory. See MPEP 2100 the 101 Guidelines.

8. As to claim 21, claim 21 recites control logic for storing data on a stack in response to the push and pop commands. However, practical application of the pushing and popping the data can be found in the claim. As to hardware –based multi-threaded processor, see discussions above. As to the control logic, control logic is an abstract idea.

9. As to claims 29, 30, the computer readable medium is not limited to hardware [CD-ROMs] but also includes carrier wave (see paragraph 0041). Therefore, not statutory. Furthermore, computer logic is non-functional descriptive material. Non-functional descriptive material in a storage is not statutory (see MPEP 2100). As the

hardware –based multi-threaded processor, see discussions above. As to the computer executable instructions causing a processor to store and retrieve data, it is intended use, not positive recitation of the limitations.

10. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re LongL 759 F.2d 887,225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. Claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,631,462. Although,

the conflicting claims are not identical, they are not patentably distinct from each other because while patented claim 1 did not recite the hardware-based multi-threaded processor, one of ordinary skill in the art should be able to recognize the pushing and popping the datum (patented claim 1, lines 2-7) should have included the memory pointer for identify the memory locations, which was applicable in hardware implementation.

12. Claim 2 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,631,462. Although, the conflicting claims are not identical, they are not patentably distinct from each other because while patented claim 2 did not recite the hardware-based multi-threaded processor, one of ordinary skill in the art should be able to recognize the determination of a pointer (patented claim 2, line 4, see also the execution of the first thread in line 2) should have included the memory location, which was applicable in hardware implementation.

13. Claim 14 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 14 of U.S. Patent No. 6,631,462. Although the conflicting claims are not identical, they are not patentably distinct from each other because Although, the conflicting claims are not identical, they are not patentably distinct from each other because while patented claim 14 did not recite the hardware-based multi-threaded processor, one of ordinary skill in the art should be able to recognize the pushing and popping the datum (patented claim 14, lines 4-9, see also threads in line 2) should have included the memory pointer for identify the memory locations, which was applicable in hardware implementation.

14. Claim 21 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 21 of U.S. Patent No. 6,631,462. Although

the conflicting claims are not identical, they are not patentably distinct from each other because while patented claim 21 did not recite the hardware-based multi-threaded processor, one of ordinary skill in the art should be able to recognize the stack structure (patented claim 21, line 4) should have included the memory pointer as hardware component for identify the memory locations, which was applicable in hardware implementation.

15. Claim 29, 30 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 21 of U.S. Patent No. 6,631,462.

16. Although the conflicting claims are not identical, they are not patentably distinct from each other because although patented claim 21 did not specifically show that his push and pop commands were the processing commands as claimed in current claim 29, one of ordinary skill in the art should be able to recognize the pop and push command could be applicable for processing thread commands because patented claim 21 also taught the commands from at least tow processing threads, which was the suggestion of the use of the processing commands. Although patented claim 21 did not clearly recites the storage or retrieval of data from the first/second processing threads by executing the instruction to push/pop, patented claim 21 did disclose the Push and pop operations and the commands form the processing threads (see claim 21). Therefore, one of ordinary skill in the art should be able to recognize the storing/retrieving the data from processing thread by executing the instruction push/pop. As to the newly amended hardware based multi-threaded processor, one of ordinary skill in the art should be able to recognize the computer readable medium (patented claim 29, line 2, claim 30, line 2) should have included a memory pointer as hardware component for identify the memory locations, which was applicable in hardware implementation.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 1, 6-10,11-16,19-22-25,27,28,29,30 are rejected under 35 U.S.C. 103(a) as being unpatentable over LeBlanc et al. (5,542,070) in view of Panwar et al. (5,838,988).

18. As to claim 1, LeBlanc disclosed a method including at least :

a) pushing a datum onto a stack [return stack] by a first processing thread (see the thread xcolon in co1.10, lines 7-18);
b) popping the datum off the stack [return stack] by a second processing thread [xsemocolon] (e.g. see co1.10, lies 19-23).

19. LeBlanc did not specifically show the hardware based multithreaded processor as clamed. However, Panwar taught a hardware supported multithreaded processor (see col.12, lines 62-67, col.13, lines 1-11). It would have been obvious to one of ordinary skill in the art to use Panwar in LeBlanc for including the hardware based multithreaded processor as claimed because the use of Panwar could provide LeBlanc the ability to adapt to different type of processing construct, such as the hardware supported multithreaded processing, and it cold readily achieved by pre configuring the hardware multithreaded processor of Panwar into LeBlanc with modified system parameters (e.g. the write or read ports) so that specific hardware based process of Panwar could be recognized by LeBlanc, and because LeBlanc also taught a buffer pointer [IP] pushed onto the stack (see. Co1.10, lines 7-12)., which was a suggestion of

the applicability of the hardware based processing, such as the buffer, in doing so provided a motivation.

20. As to claims 6, 9, LeBlanc also included at least pop command for the second thread (e.g. see co1.10, lies 19-23), and retrieving the pointer to previous stack (see the popped return value in co1.10, lines 20-28), and assigned the pointer to current stack (see the current IP value in co1.10, lines 7-18).

21. As to claim 7, see the current IP value in co1.10, lines 7-18.

22. As to claim 8, LeBlanc also taught sum of the offset and the value of the current pointer
(see col.8, lines 39-49).

23. As to claim 10, LeBlanc also included the buffer pointer [IP] pushed onto the stack (see. Co1.10, lines 7-12).

24. As to claim 11, LeBlanc also included popped datum (see the popped return value in co1.10, lines 20-28).

25. As to claim 12, LeBlanc also included a third processing thread for pushing a second datum (e.g. see xxdoes in co1.11, lines 9-33).

26. As to claim 13, LeBlanc also included a third processing thread for popping a second datum (see the method in co1.16, lines 5-11).

27. As to claim 14, LeBlanc disclosed at least :

a)stack module (see the combination of the threads and the stack) that stores data by pushing it onto a stack (see co1.10, lines 7-18, see also co1.11, lines 8-30), and processing threads can retrieve information by popping the information off the stack (e.g. see co1.10, lines 19-28);

b)first processing thread [xcolon] having a first command for pushing data into stack (e.g. see co1.10, lines 7-18);

c)second processing thread [xsemicolon] having a command set (see fig.4) including at least one command for popping data off the stack (e.g. see co1.10, lines 19-28).

28. LeBlanc did not specifically show the hardware based multithreaded processor as clamed. However, Panwar taught a hardware supported multithreaded processor (see col.12, lines 62-67, col.13, lines 1-11). It would have been obvious to one of ordinary skill in the art to use Panwar in LeBlanc for including the hardware based multithreaded processor as claimed. See reasons of obviousness in Paragraph 19 above.

29. As to claims 15,16, neither applicant's claim nor the specification defined the meaning of "processing engine", therefore, the "processing engine" is assumed to be a system which is capable of executing a single task and multiple tasks. Applicant is welcome to provide his feedback or amend the claim in the next response. And, based on this assumption, LeBlanc's threads were also applicable in either single processing engine and separate processing engines because it is capable of processing each separate task in a multitasking system and established the bindings among them (see the execution of the multiple tasks in LeBlanc in col. 3, lines 55-64).

30. As to claims 19, the push and pop commands are also processor and system instructions because they were used to be executed for the operation of system in the processor.

31. As to claim 20, a bus interface of some type has to be implemented between the threads and stack module of LeBlanc, or else, the system would not work.

32. As to claim 21, LeBlanc also included at least control logic that responds to commands from at least two processing threads (co1.10, lines 7-28), the control logic storing datum on a stack structure in response to a push command (co1.10, lines 7-18) and retrieving datum from the stack in response to a pop command (e.g. see col. 10,lines 19-28).

33. LeBlanc did not specifically show the hardware based multithreaded processor as clamed. However, Panwar taught a hardware supported multithreaded processor (see col.12, lines 62-67, col.13, lines 1-11). It would have been obvious to one of ordinary skill in the art to use Panwar in LeBlanc for including the hardware based multithreaded processor as claimed. See reasons of obviousness in Paragraph 19 above.

34.

35. As to claim 22,24 LeBlanc also included the most recent stored datum (see the current IP value in co1.10, lines 7-18).

36. As to claim 23, LeBlanc also taught a pointer associated with a second datum which was stored on the stack prior to the first datum (see the push of ip-1 location in fig.5).

37. As to claim 25, a stack pointer has to be a register in some forms, or else, it will not record the pointer value.

38. As to claims 27,28, the push and pop commands are also processor and system

instructions because they were used to be executed for the. operation of system in the processor.

39. As to claim 29, LeBlanc disclosed a stack module (e.g. see the system in the higher level in fig.1) configured to store data from first processing thread by pushing the data onto a stack [return stack] (see co1.10, lines 7-18) and to retrieve the data for a second processing thread by popping the data off the stack (see col.10, lines 19-28), the stack module being responsive to a first processing thread command (see the pushin co1.10, lines 7-18) to store data on the stack [return stack] and a second processing thread command (see the pop in co1.10, lines 19-28) to retrieve data from the stack.

40. As to claim 30, LeBlanc disclosed a computer executable medium system to store data from a first processing thread by executing an instruction to push the data onto a stack [return stack] (see the push in co1.10, lines 7-18) and retrieve the data for

a second processing thread by executing an instruction to pop the data from the stack for use by second thread (e.g. see the pop in "co1.10, lines 19-28).

41. Claims 2,3 are rejected under 35 U.S.C. 103(a) as being unpatentable over LeBlanc et al. (5,542,070)) in view of Panwar et al. (5,838,988) as applied to claim 1 above, and further in view of Drimak (3,889,243).

42. As to claim 2, limitations of the parent claim have been discussed in previous paragraphs. Neither LeBlanc nor Panwar specifically taught the step of producing a pointer associated with the determined location the pointer to the current datum as clamed. However, Drimak taught the step of producing a pointer (see fig.4 150) associated with the determined location the pointer to the current datum (see the current data being pushed or popped at associated hi and lo location in co1.7, lines 10-68, col.8; lines 1-10, see also the popping instruction in the col.8, lines 14-65)/. It would have been obvious to one of ordinary skill in the art to use Drimak in LeBlanc for producing a pointer associated with the determined location the pointer to the current datum as clamed because the use of Drimak could provide LeBlanc the ability to accept particular pointer value with respect to the argument specified in the push or pop command of LeBlanc, and therefore, increasing the programming adaptability of LeBlanc, and because LeBlanc also taught a processing thread [xsemicolon] having a command set (see fig.4) including at least one command for popping data off the stack (e.g. see co1.10, lines 19-28), which was a suggestion of the need for producing a pointer associated with the determined location the pointer to the current datum in order to associating the pointer value, for the above reasons, provided a motivation. LeBlanc is used as primary reference because it shows clearly the pushing and popping the data by the processing threads. Drimak is used for supplementing the teaching of the producing the pointer associated with the determined location to the current stack datum.

43. As to claim 3, see the decoder unit 32 in fig.1 of Drimak.

44. Claims 4,5 are rejected under 35 U.S.C. 103(a) as being unpatentable over LeBlanc et al. (5,542,070) in view of Panwar et al. (5,838,988) as applied to claim 1 above, further in view of Drimak (3,889,243) as applied to claim 2 above, and further in view of Picket et al. (5,968,169).

45. As to claims 4,5, neither LeBlanc, Panwar, nor Drimak specifically showed the storage of an argument of the pop command in a location associated with the argument of the push command as claimed. However, Picket taught a storage (stack 250) of an argument of the pop command (return instruction as pop command) in a location (pointer TOS) associated with the argument of the push command (see call instruction as push command in co1.12, lines 3-25). It would have been obvious to one of ordinary skill in the art to use Picket in LeBlanc for the storing an argument of the pop command in a location associated with the argument of the push command as claimed because the use of Picket could provide the capability of Leblanc to map the pushed and popped data elements in a predefined sequence, and therefore increasing the control ability of the stack, and because Leblanc also taught a control logic that responded to commands from at least two processing threads (co1.10, lines 7-28), Which was a suggestion of the need for storing an argument of the pop command, such as return for threads, or the like, in a location associated with the argument of the push command, such as the calls for thread processing in order to maintain the predefined set of processing sequence, and in doing so provided a motivation.

46. Claims 17,18 rejected under 35 U.S.C. 103(a) as being unpatentable over LeBlanc et al. (5,542,070) in view of Panwar et al. (5,838,988) as applied to claims 14,16, and further in view of Dangelo (5,946,487).

47. As to claims 17,18, limitations of the parent claim were already discussed in Paragraphs above, therefore, it will not be repeated herein. Neither LeBlanc nor Panwar specifically showed his stack module and the threads were on the same integrated circuit as claimed. However, Dangelo disclosed a single integrated circuit which included a stack module (stack pointer, program counter etc.) and threads in the same memory space (e.g. see col.8, lines 7-14, co1.10, lines 25-33). It would have been obvious to one of ordinary skill in the art to use Dangelo in LeBlanc as claimed because the use of Dangelo could enhance the control ability of LeBlanc to adapt to different type of system modules, such as threads and stack modules, at a given connection of a predetermined set of structural requirements of the data processing system, thereby reducing the hardware overheads and the cost, and it could be readily achieved by predefining the interface parameters of single integrated circuit of Dangelo, such as the access read/write ports, into LeBlanc so that the single integrated circuit of Dangelo could be recognized by LeBlanc, and in doing so provided a motivation.

48. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over LeBlanc et al. (5,542,070) in view of Panwar et al. (5,838,988) as applied to claims 23 above, and further in view of Duncan (5,617,327).

49. As to claim 26, limitations of the parent claim were already discussed in Paragraphs above, therefore, it will not be repeated herein. LeBlanc did not teach the SRAM. However, Duncan taught a SRAM stack (see fig.25e). It would have been obvious to use Duncan in LeBlanc for including the SRAM location because the use of Duncan could provide LeBlanc the ability to adapt specific type of memory, and because Leblanc taught he memory usage of his threads (see fig.3), which was a suggestion of the need for providing any well known memory, such as the SRAM, to increase the ability of system memory, and since no specific type of SRAM has been reflected into the claim, SRAM in general should have been well recognized by one of ordinary skill in the art, for the above reasons, provided motivation.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

50. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Wang (5,828,881) is cited for the teaching of the well known use of SRAM stack (see the SRAM col.3, lines 5-29, co1.4, lines 25-45).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP